

CLAIMS

What is claimed is:

- 5 1. A method for look-ahead load pre-fetch,
comprising the steps of:
searching an instruction stream for a load
memory instruction while the instruction stream is
stalled waiting for completion of a previous
10 instruction in the instruction stream;
issuing a pre-fetch operation for the load
memory instruction.
- 15 2. The method of claim 1, wherein the previous
instruction is a previous load memory instruction.
- 20 3. The method of claim 1, wherein the step of
issuing comprises the step of issuing the pre-fetch
operation if a memory address for the load memory
instruction is resolved and not otherwise.
- 25 4. The method of claim 1, wherein the step of
issuing the pre-fetch operation comprises the step of
issuing the pre-fetch operation while the instruction
stream is stalled on the previous instruction.
- 30 5. The method of claim 1, wherein the pre-fetch
operation reads a set of data from a main memory and
stores the data in a cache.
6. The method of claim 1, further comprising the
steps of searching the instruction stream for a set
of additional load memory instructions and issuing a

pre-fetch operation for each additional load memory instruction having a memory address which is resolved while the instruction stream is stalled.

- 5 7. An apparatus for look-ahead load pre-fetch, comprising:

 means for searching an instruction stream for a load memory instruction while the instruction stream is stalled waiting for completion of a previous instruction in the instruction stream;

10 means for issuing a pre-fetch operation for the load memory instruction.

- 15 8. The apparatus of claim 7, wherein the previous instruction is a previous load memory instruction.

- 20 9. The apparatus of claim 7, wherein the means for issuing comprises means for issuing the pre-fetch operation if a memory address for the load memory instruction is resolved and not otherwise.

- 25 10. The apparatus of claim 7, wherein the means for issuing the pre-fetch operation comprises means for issuing the pre-fetch operation while the instruction stream is stalled on the previous instruction.

- 30 11. The apparatus of claim 7, wherein the pre-fetch operation reads a set of data from a main memory and stores the data in a cache.

12. The apparatus of claim 7, further comprising means for searching the instruction stream for a set of additional load memory instructions and means for

issuing a pre-fetch operation for each additional load memory instruction having a memory address which is resolved while the instruction stream is stalled.

- 5 13. A processor, comprising:
 instruction pipeline for executing an
 instruction stream;
 means for searching the instruction pipeline for
 a load memory instruction while the instruction
10 pipeline is stalled;
 functional unit that issues a pre-fetch
 operation for the load memory instruction.
- 15 14. The processor of claim 13, wherein the
 instruction pipeline searches the instruction
 pipeline during a stall on a load memory instruction
 in the instruction stream.
- 20 15. The processor of claim 13, wherein the
 functional unit issues the pre-fetch operation if a
 memory address for the load memory instruction is
 resolved and not otherwise.
- 25 16. The processor of claim 13, wherein the
 functional unit issues the pre-fetch operation while
 the instruction stream is stalled.
- 30 17. The processor of claim 13, further comprising a
 cache such that the pre-fetch operation reads a set
 of data from a main memory and stores the data in the
 cache.